Review on FPGA Implementation of OFDM

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Abstract- The technique of orthogonal frequency division multiplexing (OFDM) is famous for its robustness against frequency-selective fading channel. This technique has been widely used in many wired and wireless communication systems. The main objective of this paper is to study the design and implementation process involve in implementing OFDM system on FPGA.

Keywords- **OFDM, IFFT, HDL, FFT, FPGA, Cyclic Prefix (CP).**

I. INTRODUCTION

The current communication systems tend to use OFDM systems in order to provide high data rates, minimize inter symbol interference and fading effect. Some examples are Digital Video Broadcasting (DVB), Wireless USB or Wireless Firmware among others. Trying to provide a solution to the new devices emerging, slow standard adoption, poor spectrum use, etc. This work presents an FPGA design, validation and implementation of an Orthogonal Frequency Division Multiplexing (OFDM) transceiver using a high level design tool and also reports the resources requirements for the presented system. OFDM allows many users to transmit in an allocated band, by subdividing the available bandwidth into many narrow bandwidth carriers. Each user is allocated several carriers in which to transmit their data. The transmission is generated in such a way that the carriers used are orthogonal to one another, thus allowing them to be packed together much closer than standard frequency division multiplexing (FDM). This leads to OFDM providing a high spectral efficiency.

Although OFDM was first developed in the 1960s, only in recent years, it has been recognized as an communication where its implementation relies on very high-speed digital signal processing. This method has only recently become available with reasonable prices versus performance of hardware implementation.

Since OFDM is carried out in digital domain there are various way of implementing it. One way is through ASICs implementation. ASICs are the fastest and low power way to implement OFDM System. Other way is to implement the system using DSPs. They provides fast vector multiplication and flexibility in the design can be achieved. But there are some lof the obvious advantages of using both of them so designer are moving towards FPGA. An FPGA combines speed power and density advantage of ASICs and flexibility and reprogram ability general purpose processor. Hence FPGA is a best choice for OFDM system as it provides flexibility to design and provide low cost advantage. The basic OFDM system consist of QAM or PSK modulator/demodulator ,serial to parallel and parallel to serial convertor and IFFT/FFT modules.

The rest of this paper is organized as follows. Section II describes the Literature survey, OFDM theory and its Fundamental. System Design is described in section III. Hardware Description Language and FPGA are discussed in section IV. Applications of OFDM are described in section V. Section VI concludes the paper.

II. CURRENT SCENARIO

CURRENT System-on-Chip (SOC) platforms provide wide range of programmable processors and ASIC components .These components provide user, a flexibility & reduction of cost of implementation. ASIC are not suitable were flexibility is required. By implementing the OFDM using FPGA, performance can be increased.

In 2013, Nilesh Chide, *Et. Al.* [4] Proposed The Design Of OFDM System Using IFFT And FFT Blocks And Simulation Was Done On XILINX ISE. They Implemented The OFDM Block By Block And Finally Incorrect All Of Them Together To Form Complete OFDM Circuit. Finally Their Aim Is To Implement The Core Signal Processing Blocks Of OFDM System Using VHDL Language. The Different Blocks Of OFDM System Such As QAM Modulator, 8-IFFT, 8-FFT And Demodulator Is Designed On Xilinx Project Navigator. These Blocks Are Simulated On XILINX ISE Design Suite, Tested For Different Patterns And Results Are Compared.

In 2008 S. Haene, D. Perels & A Burg [2] proposed that A real-time MIMO-OFDM physical layer transmitting at a peak data rate of 216Mbit/s over 20MHz bandwidth was prototyped and characterized through measurements. Real-time operation of the system on an FPGA was achieved by diligent selection and optimization of the employed transceiver algorithms for the FPGA implementation and by careful design of the corresponding transceiver hardware architecture.

In 2011 P. J. Lobo, F. Pescador, G. Maturana & M. C. Rodríguez [17] proposed that it could be possible to integrate the whole system (i.e. receiver and gateway) in a single platform with one DSP and the FPGA, especially

considering that current versions of the DSPs. A combined SoC that includes both the communications and video peripherals would be perfectly fit for the task. Other functional combinations are possible, such as a receiver and gateway without video decoding capabilities or even a system with just the gateway functionality. In the latter case, a smaller and cheaper processor could be used.

In 2012 Z. Iqbal, S Nooshabadi & Heung-No Lee [18] proposed that OFDM gives an efficient way to design the IEEE 802.16 system for FPGA. A special double-buffering design method is used to implement the interleaver with minimum memory requirement and initial latency.

III. OFDM THEORY

OFDM is an attractive modulation scheme used in broadband wireless systems that encounter large delay spreads. OFDM avoids temporal equalization altogether, using a cyclic prefix technique with a small penalty in channel capacity. Where Line-of-Sight (LoS) cannot be achieved, there is likely to be significant multipath dispersion, which could limit the maximum data rate. Technologies like OFDM are probably best placed to overcome these, allowing nearly arbitrary data rates on dispersive channels. The difference between single carrier transmission and multicarrier transmission (OFDM) shown in Fig.1 [3].

For each subcarrier a rectangular pulse shaping is applied. The guard interval or cyclic extension is added to the subcarrier signal in order to avoid intersymbol interference (ISI), which occurs in multipath channels as shown in Fig.2. At each receiver the cyclic prefix is removed and only the time interval [0,Ts] is evaluated. The spectra of the subcarriers overlap, but the subcarrier signals are mutually orthogonal, and the modulation symbol can be recovered by a simple correlation as shown in Fig.3 [3].
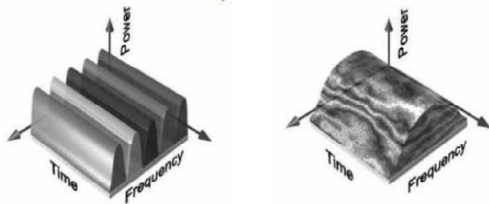

Figure 1. Single carrier versus multicarrier transmission

A. Orthogonality

The key to OFDM is maintaining orthogonality of the carriers. If the integral of the product of two signals is zero over a time period, then these two signals are said to be orthogonal to each other. Two sinusoids with frequencies that are integer multiples of a common frequency can satisfy this criterion. Therefore, orthogonality is defined by:

$$\int_a^b \emptyset_n(t)\emptyset'_m(t)dt = 0; n \neq m$$

where n and m are two unequal integers; f_o is the fundamental frequency; T is the period over which the integration is taken. For OFDM, T is one symbol period and f_o set to $1/T$ for optimal effectiveness [5].

B. Advantages of OFDM

In general, OFDM systems have the following advantages:(i) makes efficient use of the spectrum by allowing overlap; (ii) By dividing the channel into narrowband flat fading subchannels, OFDM is more resistant to frequency selective fading than single carrier systems are; (iii) Eliminates ISI and IFI through use of a cyclic prefix; (iv) using adequate channel coding and interleaving one can recover symbols lost due to the frequency selectivity of the channel; (v) channel equalization becomes simpler than by using adaptive equalization techniques with single carrier systems; (vi) It is possible to use maximum likelihood decoding with reasonable complexity; (vii) OFDM is computationally efficient by using FFT techniques to implement the modulation and demodulation functions; (viii) Is less sensitive to sample timing offsets than single carrier systems are, and (ix) provides good protection against cochannel interference and impulsive parasitic noise [2,3].

C. Disadvantages of OFDM

OFDM systems have the following disadvantages: (i) High synchronism accuracy; (ii) Multipath propagation must be avoided in other orthogonality not be affected, and (iii) Large peak-to-mean power ratio due to the superposition of all subcarrier signals, this can become a distortion problem.[2,3]
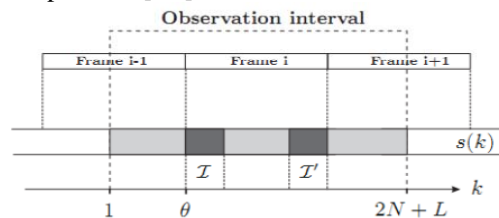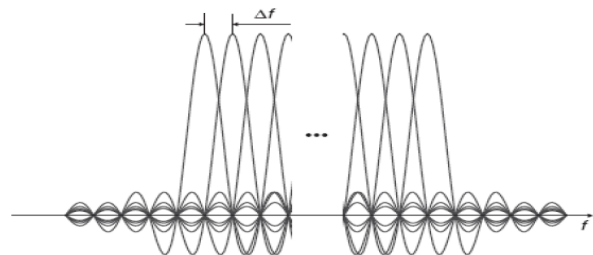

Fig. 2 Cyclic Extension

Fig. 3 OFDM subcarriers representation

IV. IFFT/FFT PROCESSOR

Different hardware architectures have been used in the literature for the implementation of the CT algorithms. The FFT hardware architectures can be classified into three groups:
• Monoprocessor: A single hardware element is used to perform all the butterflies, twiddle factor multiplications and data shuffling of each stage. The same hardware is reused for all the stages.
• Parallel: The computation of the butterflies, twiddle factor multiplications and data shuffling within one stage is accelerated by using several processing elements. The same hardware elements are again reused for all the stages.

• Pipeline: A single hardware element is used to perform all the butterflies, twiddle factor multiplications and data shuffling of each stage. However, in contrast to former categories, a different hardware element is used to process each stage.[1,3]

Different kinds of FFT algorithms can be found in the literature; e.g.: (Good, 1958; Thomas, 1963), (Cooley & Tukey, 1965), (Rader, 1968b), (Rader, 1968a), (Bruun, 1978) and (Winograd, 1978). Among the different kinds of FFT algorithms, the algorithms based on the approach proposed by James W. Cooley and JohnW. Tukey in (Cooley & Tukey, 1965) are very popular in OFDM systems.[1]

These Cooley–Tukey (CT) algorithms present a very regular structure, which facilitates an efficient implementation. N-point IFFT/FFT modules which implement radix 2 Cooley–Tukey algorithm perform parallel computation of the even-indexed and the odd-indexed outputs, by using two interleaved N/2-point IFFT/FFTs. This approach allows recursive algorithm execution in log2N phases. In each phase the input data sequence is divided into two N/2 point data sequences, allowing parallel "butterfly" processes to be performed, computing sums or differences for the symbols of the first and the second half of the input signal, respectively. The odd-numbered samples of the IFFT/FFT require the pre-multiplication of the input sequence with a so-called twiddle/conjugated twiddle factors, accordingly. For illustrative purposes, an 8-point radix 2 Cooley–Tukey FFT computation is shown in figure 4.

Before going further to discuss on the FFT and IFFT design, it is good to explain a bit on the Fast Fourier Transform and Inverse Fast Fourier Transform operation. The Fast Fourier Transform (FFT) and Inverse Fast Fourier Transform (IFFT) are derived from the main function which is called Discrete Fourier Transform (DFT). The idea of using FFT/IFFT instead of DFT is that the computation of the function can be made faster where this is the main criteria for implementation in the digital signal processing. In DFT the computation for N-point of the DFT will calculate one by one for each point. While for FFT/IFFT, the computation is done simultaneously and this method saves quite a lot of time. Below is the equation showing the DFT and from here the equation is derived to get FFT/IFFT function.

$$X(k) = \sum_{n=0}^{N-1} x(n)e^{-j2\pi nk/N}$$
(4.1)

$X(k)$ represent the DFT frequency output at the *k*-the spectral point where k ranges from 0 to *N-1*. The quantity *N* represents the number of sample points in the DFT data frame. The quantity *x(n)* represents the *n*-th time sample, where *n* also ranges from 0 to *N-1*. In general equation, *x(n)* can be real or complex.

The DFT equation can be re-written into:

$$X(k) = \sum_{n=0}^{N-1} x(n)W_N^{nk}$$
(4.2)

The quantity W_N^{nk} is defined as:

$$W_N^{nk} = e^{-j2\pi nk/N}$$
(4.3)

Here is where the secret lies between DFT and FFT/IFFT where the function above is called Twiddle Factor. This factor is calculated and put in a table in order to 37 make the computation easier and can run simultaneously. The Twiddle Factor table is depending on the number of point use. During the computation of IFFT, the factor does not to recalculate since it can refer to the Twiddle factor table thus it save time since calculation is done concurrently. Below is the table for 8 point of FFT for twiddle factor.

For decimation in frequency radix-2, the input is separated into two halves which is:

$$x(0), x(1), \ldots, x\left(\frac{N}{2}-1\right)$$
(4.4)

And

$$x\left(\frac{N}{2}\right), x\left(\frac{N}{2}+1\right), \ldots, x(N-1)$$
(4.5)

Thus the DFT also can be separated into two summations:

$$X(k) = \sum_{n=0}^{(N/2)-1} x(n)W^{nk} + W^{kN/2} + \sum_{n=N/2}^{N-1} x(n)W^{nk}$$
(4.6)

Substituting the input into equation above, the result is:

$$X(k) = \sum_{n=0}^{(N/2)-1} x(n)W^{nk} + W^{kN/2} \sum_{n=0}^{(N/2)-1} x\left(n+\frac{N}{2}\right)W^{nk}$$
(4.7)

Substituting k = 2k for even and k = 2k + 1 for odd the equation become as:

$$X(2k) = \sum_{n=0}^{(N/2)-1}\left[x(n) + x\left(n+\frac{N}{2}\right)\right]W^{2nk}, \quad k = 0,1,\ldots,\left(\frac{N}{2}\right)-1$$
(4.8)

And

$$X(2k+1) = \sum_{n=0}^{(N/2)-1}\left[x(n) - x\left(n+\frac{N}{2}\right)\right]W^n W^{2nk}, \quad k = 0,1,\ldots,\left(\frac{N}{2}\right)-1$$
(4.9)

Furthermore, let:

$$a(n) = x(n) + x\left(n+\frac{N}{2}\right)$$
(4.10)

$$b(n) = x(n) - x\left(n+\frac{N}{2}\right)$$
(4.11)

To equation ….:

$$X(2k) = \sum_{n=0}^{(N/2)-1} a(n)W_{N/2}^{nk}$$
(4.12)

$$X(2k+1) = \sum_{n=0}^{(N/2)-1} b(n)W_{N/2}^{nk}$$
(4.13)

The equation above shows that for FFT decimation in frequency radix 2, the input can be grouped into odd and even number. Thus, graphically the operation can be view using FFT flow graph shown in figure.

From this figure, the FFT computation is accomplished in three stages. The X(0) until X(7) variable is denoted as the input value for FFT computation and Y(0) until Y(7) is denoted as the output. There are two operations to complete the computation in each stage. The upward arrow will
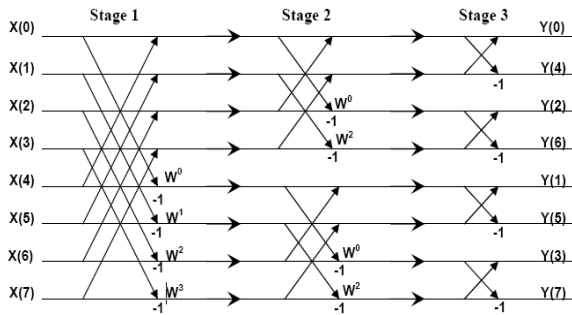

Figure. 4-point FFT flow graph using decimation-in-frequency (DIF).

execute addition operation while downward arrow will execute subtraction operation. The subtracted value is multiplied with twiddle factor value before being processed into the nest stage. This operation is done concurrently and is known as butterfly process. For second stage, there are two butterfly process with each process get reduced input variable. In the first stage the butterfly process get eight input variable while in the second stage, each butterfly process get four input variable that is from first stage computation. This process is continued until third stage. In third stage, there are four butterfly processes. Noted that each of the butterfly process is performed concurrently enable it to execute FFT computation process in a very fast technique.

V. HDL AND FPGA IMPLEMENTATION

Since OFDM is carried out in the digital domain, there are several methods to implement the system. One of the methods to implement the system is using ASIC (Application Specific Integrated Circuit). ASICs are the fastest, smallest, and lowest power way to implement OFDM into hardware. The main problem using this method is inflexibility of design process involved and the longer time to market period for the designed chip. Another method that can be used to implement OFDM is general purpose Microprocessor or Micro Controller. Power PC 7400 and DSP Processor is an example of microprocessor that is capable to implement fast vector operations. This processor is highly programmable and flexible in terms of changing the OFDM design into the system. The disadvantages of using this hardware are: it needs memory and other peripheral chips to support the operation. Besides that, it uses the most power usage and memory space, and would be the slowest in terms of time to produce the output compared to other hardware.

Field-Programmable Gate Array (FPGA) is an example of VLSI circuit which consists of a "sea of NAND gates". This hardware is programmable and the designer has full control over the actual design implementation without the need (and delay) for any physical IC fabrication facility. An FPGA combines the speed, power, and density attributes of an ASIC with the programmability of a general purpose processor will give advantages to the OFDM system. An FPGA could be reprogrammed for new functions by a base station to meet future needs particularly when new design is going to fabricate into chip. This will be the best choice for OFDM implementation since it gives flexibility to the program design besides the low cost hardware component compared to others.

HDL stands for Hardware Description Language which is used to describe any digital hardware from gates to microprocessor assembly in the form of high level programming. HDL can define any hardware at any level. Designer can use either Top-Bottom or Bottom-Up approach for hardware description. For design with increasing complexity as in our case of OFDM we generally prefer Top-Bottom approach. Verilog HDL is used in this project for design description at various level of abstraction (1) Behavioral (2) Data Flow or RTL (3) Gate Level. Verilog provide flexibility of using different level of abstraction in same module. Hardware architecture for the proposed design was developed, realized in Verilog. The realized architectures was tested and validated the outputs are generated by a hardware simulation using Modelsim.[4]
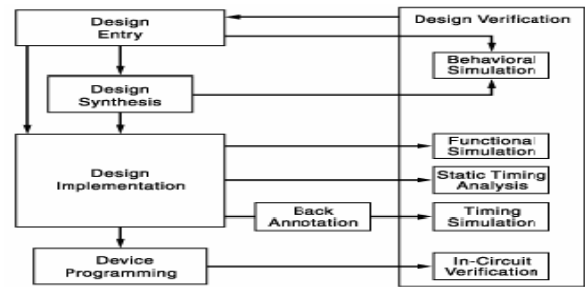

Figure 5 . FPGA Design Flow

Field Programmable Gate Arrays (FPGAs) are semiconductor devices that are based around a matrix of configurable logic blocks (CLBs) connected via programmable interconnects. FPGAs can be reprogrammed to desired application or functionality requirements after manufacturing. This feature distinguishes FPGAs from Application Specific Integrated Circuits (ASICs), which are custom manufactured for specific design tasks.[4]

Once the simulation results are verified next process is to perform synthesis to generate a gate level net list of the designed hardware. The realized hardware description is synthesized using Xilinx. Spartan 3E FPGA board is used for synthesis and verifying design on FPGA board.

VI. APPLICATIONS OF OFDM

It has emerged as the leading physical-layer interface in wireless communications in the last decade. OFDM has been widely studied in mobile communications

to combat hostile frequency selective fading and has been incorporated into wireless network standards (802.11a/g Wi-Fi, HiperLAN2, 802.16 Wi MAX) and digital audio and video broadcasting (DAB and DVB-T) in Europe, Asia, Australia, and other parts of the world.

VII. CONCLUSION

The main objective is to study all the core processing block of OFDM. Among all the block IFFT/FFT block are of great importance as it provide the necessary conversion of signal from time to frequency domain and vice versa and provides orthogonality to signal. IFFT/FFT is used instead of DFT/IDFT because of the advantage of high computational capability and less computational time of the former. Cyclic prefixes are added at the transmitted signal to preserve orthogonality and to provide time and frequency synchronization. Hardware Description of design is done in Verilog HDL. Hence all the aspect of OFDM from its theory to actual implementation is studied in detail.

The proposed algorithm and architecture should be validated by MATLAB simulation before implementation. After that, it is implemented with VHDL.

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